Study of Thermal Noise of SGMOSFET with Different Substrate and Gate Oxides

Saradindu Panda¹, Chiradeep Mukherjee², Prof.B.Maji³ and Prof.A.K.Mukhopadhyay⁴

¹Electronics & Communication Engineering Department, Narula Institute of Technology, Kolkata, India
²Electronics & Communication Engineering Department, Institute of Engineering & Management, Kolkata, India
³H.O.D, Electronics & Communication Engineering Department, NIT, Durgapur, India
⁴Director, BITM, Santiniketan, India

Abstract: In improving field of Metal Oxide Semiconductor technology (MOS-technology), highly gate controllable structures are continuously developed in research labs. With increased controllability of gate, the size of the semiconductor devices is also decreasing. Similarly in MOS physics, the channel length has been decreased below 0.1µm but with MOSFET scaling various important parameters have to be analyzed whether they are showing Quantum effects or not. To understand the overall picture of thermal noise performance of SGMOSFET the short channel parameters such as length, radius of gate, working temperature, doping concentration and the other parameters varied. These results shaped by different simulation results can be taken as standard and optimum device constraints. By having these data we can understand which configurations are giving the best thermal noise performance under the same set of parameters-related simulation environment. In this paper we give the thermal noise performance of various substrates with respect to different oxides and propose best cases.

Keywords: Thermal-Noise formulation, SGMOSFET

1. INTRODUCTION

We have seen the modeling of noise in case of Surrounding Gate MOSFET (SGMOSFET) in our previous work [1]. These devices are manufactured in different research laboratory. But growing technology gives silicon arena the several complexities. Different data simulators use the data to implement several analytical models. We retrospect the model for analysis of noise in case of SGMOSFET. In this paper, we represent comparative noise analysis in case of modeling of thermal noise for SGMOSFET.

We use an analytical model where N_a is the acceptor concentration N_a in the silicon layer with thickness equal to t_ox; t_ox is the equivalent gate oxide thickness; and the radius of the cylinder is R.

2. ANALYTICAL NOISE MODELING

In our previous work, we modeled the Thermal noise Behavior of SGMOSFET [1]. The expression for power spectral density is given by:

\[ S_{th} = \frac{V_r}{L} \int_{0}^{\infty} \frac{g^2(V, E)}{g(V, E)} S_{ch} dV \]  

(1)

The drain current for SGMOSFET is given by

\[ I_D = \frac{2 \pi R_{D}}{L} \left[ 2V_t(Q_s, Q_v) \cdot \frac{Q^2 - Q_0^2}{2C_m} \right] \]

+ \[ V_c Q_s \log \left( \frac{Q_0}{Q_s} \right) \]

(2)

Here Q_s is the mobile charge density per unit area and Q_0 is Q at the drain end. The expression for the charge sheet density per unit area is given by:

\[ Q = Q_{si} \left( \frac{2C_m V_s^2}{Q_s} \right) \left[ \frac{4V_t^3}{\log^2 \left( 1 + \exp \left( \frac{V_{gs} - V_{th} - V}{2V_t} \right) \right)} \right] \]

(3)

We need another expression of inverse charge for calculating the Threshold voltage as:

\[ Q' = Q_{ox} \left( \frac{2C_m V_s^2}{Q_s} \right) \frac{4V_t^3}{\log^2 \left( 1 + \exp \left( \frac{V_{gs} - V_{th} - V}{2V_t} \right) \right)} \]

(4)

Lastly threshold voltage expression is given as:

\[ V_{th} = V_0 + 2V_t \log \left( 1 + \frac{Q}{2Q_0} \right) \]

\[ \Delta V_a = \frac{C_m V_s}{Q_a} \left( \frac{Q}{Q_0} \right) \frac{Q_0}{\frac{Q}{2}} \]

(5)

\[ V_{th} = \Delta V_a + \frac{qN_a R}{C_m} + \frac{qN_a}{2C_m} \cdot V_t \cdot \ln \left( \frac{8}{\pi^2} \right) \]

(6)

Where \( C_m \) and \( \delta \) are given by:

\[ C_m = \frac{\varepsilon_m}{R \ln(1 + t_{ox}/R)} \] and

\[ \delta = \frac{qN_a}{V_t} \frac{1}{2C_m} \]
Here \( q \) is electronic charge, \( n_i \) being the intrinsic carrier concentration, \( \varepsilon_i \) is the permittivity of silicon, \( C_{si} \) is the silicon capacitance and \( C_{ox} \) is the oxide capacitance, \( \mu \) is the effective mobility[2]. \( R \) is effective radius of cylindrical surface of the device and finally \( L \) is the channel length.

In this paper we have taken an n-type SGMOSFET. We make a comparative study by taking Si-substrate & GaAs-substrate with different oxides. For each observation we take Si-substrate along with SiO\(_2\) as oxide, then Si3N4 as oxide and finally alumina as oxide. We repeat the same observations by taking GaAs-substrate with the same oxides as above. In each case we vary channel length \( L \), Channel Radius \( R \), Doping Concentration \( N_a \) and operating temperature.

3. COMPARATIVE RESULT ANALYSIS

Title and authors

We consider here Silicon (Si) as well as Gallium Arsenide (GaAs) as substrate. We have taken Silicon with different oxides. The oxides used here are Silicon Dioxide, Silicon Nitride and lastly Alumina.

When Radius of SGMOSFET is decreasing then Oxide capacitance increases as they are inversely related to each other. So drain current will increase as mobile charge per unit gate area is directly proportional to Oxide Capacitance. Thermal Noise Spectral Density will be decreasing as shown by the Figure 1. The Thermal Noise Power density for different oxides are shown by Figure 2.

Equation 1 shows us that Thermal noise is inversely proportional to Channel Length. So Thermal noise Spectral density \( S_{id} \) will decrease as shown in figure 3:

![Figure 1](image1.png)

**Figure 1**: Modeled Thermal Noise prior to velocity saturation for different Radius of the cylindrical substrate.

![Figure 2a](image2a.png)

**Figure 2a)**: For Silicon Substrate

![Figure 2b](image2b.png)

**Figure 2b)**: For GaAs Substrate

**Figure 2**: Modeled Thermal Noise prior to velocity saturation for different Radius of the cylindrical substrate using different oxides.

![Figure 3](image3.png)

**Figure 3**: Modeled Thermal Noise prior to velocity saturation for different Channel Length.
The Thermal Noise Power density by varying Channel Length for different oxides on different substrates is shown by Figure 4:

- Figure 4a): For Silicon Substrate
- Figure 4b): For GaAs Substrate

Figure 4: Modeled Thermal Noise prior to velocity saturation for different Channel Length of the cylindrical substrate using different oxides

When we increase the operating Temperature the Thermal Noise Spectral Density SId will be increased as shown in figure 5.

Figure 5: Modeled Thermal Noise prior to velocity saturation for different Temperature.

The Thermal Noise Power density for different oxides for different operating temperature is shown by Figure 6:

- Figure 6a): For Si Substrate
- Figure 6b): For GaAs Substrate

Figure 6: Modeled Thermal Noise prior to velocity saturation for different Operating Temperature using different oxides

When we increase the doping concentration then mobile charge (Q) per unit area will be increased. The increased Q will increase the drain current as Q and Oxide capacitance are directly proportional as a result thermal Power spectral density will decrease as shown in figure 7,8:
The observations by taking different Substrate in contrast with Silicon Dioxide, Silicon Nitride and Alumina are given by Figure 9,10,11,12. For each case we take Silicon as substrate at first and verify with aforementioned three oxides. Next we take GaAs as substrate and incorporate it with the same three oxides. For each observations, We change the parameters such as Channel Length, Radius of Channel, Operating Temperature and finally Doping Concentration.
Figure 10b): Modeled Thermal Noise prior to velocity saturation for different Radius of Channel using Silicon Nitride as Oxide

Figure 10c): Modeled Thermal Noise prior to velocity saturation for different operating temperature using Silicon Nitride as Oxide

Figure 10d): Modeled Thermal Noise prior to velocity saturation for different Doping Concentration using Silicon Nitride as Oxide

Figure 11a): Modeled Thermal Noise prior to velocity saturation for different Channel Length using Alumina as Oxide

Figure 11b): Modeled Thermal Noise prior to velocity saturation for different Radius of Channel using Alumina as Oxide

Figure 11c): Modeled Thermal Noise prior to velocity saturation for different operating temperature using Alumina as Oxide

Figure 11d): Modeled Thermal Noise prior to velocity saturation for different doping concentration using Alumina as Oxide

Figure 12a): Modeled Thermal Noise prior to velocity saturation for different Channel Length using Silicon Nitride as Oxide
Figure 12b): Modeled Thermal Noise prior to velocity saturation for different Radius of Channel using Silicon Nitride as Oxide

Figure 12c): Modeled Thermal Noise prior to velocity saturation for different operating temperature using Silicon Nitride as Oxide

Figure 12d): Modeled Thermal Noise prior to velocity saturation for different doping concentration using Silicon Nitride as Oxide

4. Conclusion
The thermal noise modeling is very important because when we make thin gate oxide then leakage current plays an important factor. So as to optimize the Thermal Noise we observe the best case where we have taken Silicon as substrate. The best cases for Silicon taken as substrate are given as Table II.

Table II: Table showing Thermal Noise Value for Si & GaAs substrate taking different varying parameters

<table>
<thead>
<tr>
<th>Substrate</th>
<th>Parameters</th>
<th>Oxide</th>
<th>Thermal Noise in $A^2/Hz$ *10$^{-10}$</th>
</tr>
</thead>
<tbody>
<tr>
<td>Si</td>
<td>R=10nm, L=50nm, $N_A=10^{16}$/cu.m., T=300K</td>
<td>Silicon Dioxide</td>
<td>1.319</td>
</tr>
<tr>
<td></td>
<td>R=5nm, L=100nm, $N_A=10^{18}$/cu.m., T=300K</td>
<td>Silicon Nitride</td>
<td>1.272</td>
</tr>
<tr>
<td></td>
<td>R=5nm, L=150nm, $N_A=10^{16}$/cu.m., T=300K</td>
<td>Alumina</td>
<td>1.107</td>
</tr>
<tr>
<td>GaAs</td>
<td>R=5nm, L=150nm, $N_A=10^{22}$/cu.m., T=300K</td>
<td>Silicon Dioxide</td>
<td>2.290</td>
</tr>
<tr>
<td></td>
<td>R=10nm, L=100nm, $N_A=10^{22}$/cu.m., T=300K</td>
<td>Silicon Nitride</td>
<td>3.079</td>
</tr>
<tr>
<td></td>
<td>R=10nm, L=100nm, $N_A=10^{22}$/cu.m., T=300K</td>
<td>Alumina</td>
<td>3.662</td>
</tr>
</tbody>
</table>

Whereas the best cases for GaAs is given as:

In our modeling we propose best configuration (R=5nm, L=150nm, $N_A=10^{16}$/m$^3$, T=300K) by taking Aluminum di-oxide as gate oxide where Silicon is used as substrate. It can also be used as circuit simulation parameters in industrial purpose to analyze the noise performance of SG MOSFET. This paper also shows the optimized modeling which will be very important and helpful for IC optimized design at low power supply.

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References


AUTHOR
Saradindu Panda
He received M.Tech from Jadavpur University in 2007 in VLSI Design and Microelectronics Technology. He is pursuing his PhD at NIT, Durgapur, West Bengal, India. Presently, he is involved in design and management of low-power and high speed integrated circuits with Solid State Devices in Nano Regime. He is now faculty in ECE Department at Narula Institute of Technology, Kolkata, India. He has more than 15 publications in different International and National Journals and Conference Proceedings.

Chiradeep Mukherjee
He is pursuing M.Tech in ECE, IEM, Kolkata, India. His research interest in the area of VLSI Low Power Design, Image Processing, Signal Processing.

Prof. (Dr.) Bansibadan Maji
He is now a senior Professor of ECE Department in NIT, Durgapur, West Bengal, India. He is now Head of The Department of ECE at NIT. His main research area on Microwave, Antenna, VLSI Design and Low power Device and Circuits. He has more than 56 publications in different International and National Journals and Conference Proceedings.

Prof. (Dr.) A. K. Mukhopadhyay
He received M.Tech from IIT, Kharagpur, and Ph.D(Engg) from Jadavpur University, India. Currently, he is the Director of BITM, Santiniketan, Birbhum, West Bengal, India. He was the Principal of BCET, Durgapur. Previously he served as the Dean (Academic) and Head of Department of ECE, Dr. B. C. Roy Engineering College, Durgapur. He also worked at Narula Institute of Technology, Kolkata, College of Engineering & Management, Kolaghat, NERIST, Itanagar and IIT, Kharagpur. His current area of research includes Wireless and Mobile Networks and Overlay-based heterogeneous networks. He has 48 publications mostly in international journal and conference proceedings. He is a Life Fellow of the Institution of Engineers (I), Member, IEEE, Member, IEEE ComSoc, Global Member, ISOC; Sr. Life Member, CSI; Life Member, ISTE, IETE, SSI etc.